

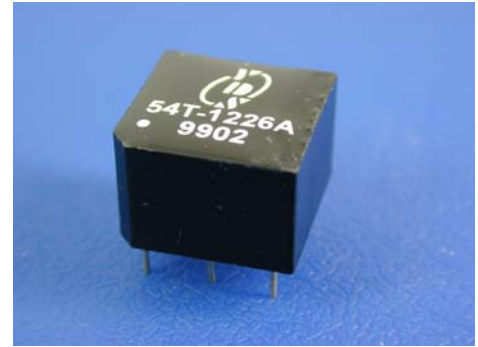


FEATURES

- FOR T1 / CEPT LINE INTERFACES
- MATCHED TO LEADING TRANSCEIVER ICs
- DESIGNED TO MEET ITU-T G.703
- RECOGNIZED BY UL 1950.

TEST CONDITIONS

- Inductance ----- 1KHz/10mV
- Leakage Inductance ----- 100KHz/200mV
- Interwinding Capacitance -- 100KHz/200mV

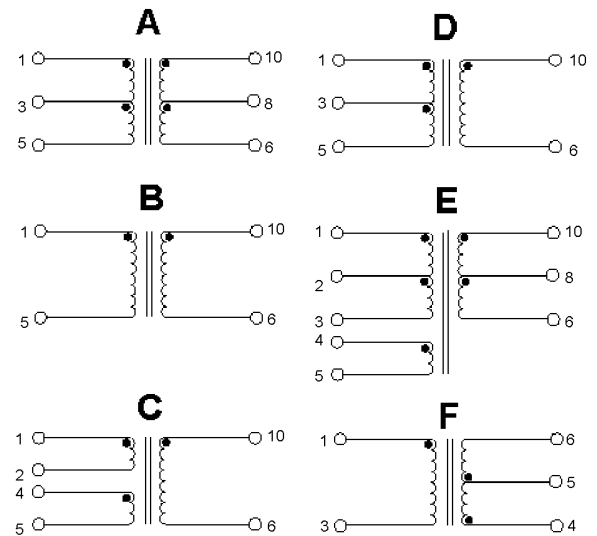
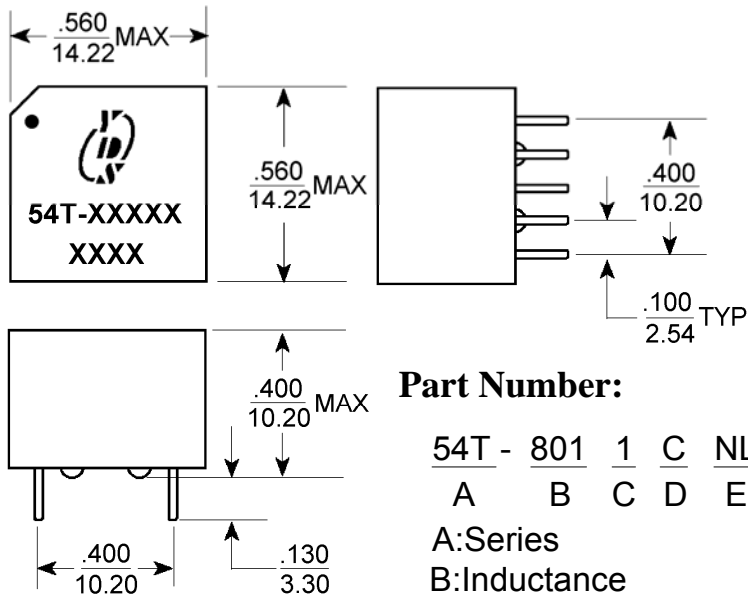


ELECTRICAL SPECIFICATIONS @25°C - Operating temperature 0°C TO 70°C (Unless Otherwise Noted)

PART NUMBER	TURNS RATIO ±5%	OCL (mH MIN)	LL (μH MAX)	Cw/w (pF MAX)	DCR PRI (Ω MAX)	DCR SEC (Ω MAX)	PACKAGE/ SCHEMATICS	PRIMARY PINS
54T-8011C	1.27CS:1	0.80	0.70	15	0.50	0.35	C	1-5
54T-8012C	1CS:1	0.80	0.70	15	0.50	0.45	C	1-5
54T-1221D	1:1.36CT	1.20	0.60	35	0.70	0.90	D	10-6
54T-1221A	1CT:2CT	1.20	0.30-0.55	20	0.50	0.90	A	1-5
54T-1221B	1:1	1.20	0.50	20	0.50	0.50	B	1-5
54T-1222A	1CT:2CT	1.20	0.80	15	0.70	1.10	A	1-5
54T-6011E	1CT:3CT:1	0.60	0.80	30	0.70	1.70	E	1-3
54T-1522D	1:1.08/1.36	1.50	0.60	20	0.70	0.90	D	10-6
54T-1523D	1:1.14CT	1.50	1.00	30	0.70	0.90	D	10-6
54T-1524D	1:1/1.26	1.50	0.60	35	0.70	1.10	D	10-6
54T-1525D	1:1.58/2	1.50	0.70	20	0.70	1.20	D	10-6
54T-1223A	1CT:1.41CT	1.20	0.80	20	0.60	0.80	A	10-6
54T-2221F	1:2CT	2.00	0.60	35	1.50	-	F	1-3

MARKINGS AND DIMENSIONS

SCHEMATICS



Dimensions: inches/mm

Unless otherwise specified, all tolerances are ±.010/±0.25